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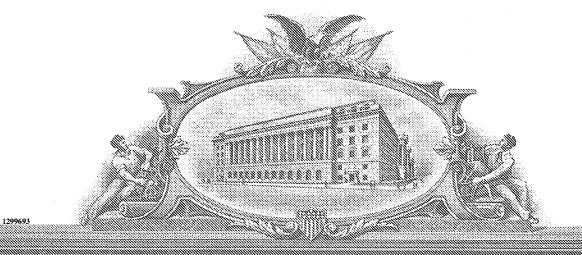
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UNITED STATES DEPARTMENT OF COMMERCE

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March 22, 2005

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APPLICATION NUMBER: 60/529,166 FILING DATE: December 12, 2003

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Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c). EU352262915US Express Mail Label No.

INVENTOR(S)						
Given Name (first and middle [if any]		Family Name or Sumame		Residence (City and either State or Foreign Country)		
David		Okada		Chandler, Arizona		
Additional inventors are being named on theseparat			separately numbe	y numbered sheets attached hereto		
TITLE OF THE INVENTION (500 characters max)						
Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards						
Direct all correspondence to: CORRESPONDENCE ADDRESS						
Customer Number: 24964					1	
OR						
Firm or Individual Name						
Address						
Address						
City			State	Zip		
Country			Telephone	Fax		
ENCLOSED APPLICATION PARTS (check all that apply)						
Specification Number of Pages 4 CD(s), Number CD(s), Numbe						
METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT						
Applicant claims small entity status. See 37 CFR 1.27. A check or money order is enclosed to cover the filing fees.				FILING FEE Amount (\$)		
The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number:				\$80.00		
Payment by credit card. Form PTO-2038 is attached.						
The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government. No. Yes, the name of the U.S. Government agency and the Government contract number are:						
[Page 1 of ∜] Respectfully submitted, Date /2/12/03					3	
SIGNATURE Will Hand				REGISTRATION NO. 36,169		
TYPED or PRINTED NAME William Havang				(if appropriate) Docket Number: 104023-135820		

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

TELEPHONE 973-992-1990

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Provisional Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Application No.

:

not yet assigned

Filing Date : First Named Inventor :

not yet assigned David Okada

Attorney Docket No.:

104023-135820

Title

Semiconductor Die with Solderable Metal System Allowing

Direct Surface Mounting to Printed Circuit Boards

CERTIFICATE OF EXPRESS MAILING

EXPRESS MAIL Mailing Label Number: EU352262915US

Deposited: December 12, 2003

I hereby certify that this and the enclosed paper(s) and/or fee(s) is/are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Commissioner for Patents; P.O. Box 1450, Alexandria, VA 22313-1450, Mail Stop Provisional Application.

Submitted herewith are the following items:

- 1) Provisional Application for Patent Cover Sheet (and duplicate): 2 pages;
- 2) Specification: 4 pages;
- 3) Drawings: 4 sheets (Figs. 1-4);
- 4) Duplicate Drawings (in color): 4 sheets (Figs. 1-4)
- 5) Certificate of Express Mailing: 1 page;
- 6) Return Receipt Postcard

Vvette Alvarez-Perez

TITLE

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

FIELD OF THE INVENTION

This invention generally relates to semiconductor technologies. This invention can be applied to all types of semiconductor die, such as integrated circuits, discrete semiconductor devices, sensors, micro-machined structures, etc.

DESCRIPTION OF THE INVENTION

The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto. Use of absolute terms, such as "will not," "will," "shall," "shall not," "must," and "must not," are not meant to limit the present invention as the embodiments disclosed herein are merely exemplary.

Typical surface mountable semiconductor components consists of a semiconductor die attached to a lead frame, wire bonded, and encapsulated into a plastic package with exposed leads. Soldering the leads to the printed circuit board provides mechanical, thermal, and electrical connections to the semiconductor die.

A typical wire bonded die is shown in Figure 1. Wire bonds add parasitic inductance and series resistance to the electronic component/circuit. The added inductance and resistance is undesirable for many devices, including high frequency devices, high speed devices, and low on-resistance power semiconductor devices. The lead frame provides the primary thermal conduction path for the die. The length of the thermal path to the printed circuit board and lead frame design and composition limits the thermal performance of a package.

Wire bonds and lead frames can be eliminated using flip chip wafer bumping packaging. Examples of two available flip chip processes are shown in Figure 2. Additional processing is performed to the top surface of the semiconductor die to attach a solder ball or build a raised conductive region with a top coating of solder. This allows the device to be attached to the printed circuit board. A disadvantage of the solder ball approach is the limited contact area of the ball to the die surface and printed circuit board. This reduces both the thermal and electrical conduction areas increasing both the thermal and electrical resistance. The thermal and electrical paths are long, approximately the diameter of the solder ball. The limited contact area of the ball also results in the limited mechanical strength of the bond between the die and printed circuit board.

The copper pedestal bump is an improvement over the solder ball. Current and heat flows through copper which is significantly more thermally and electrically conductive

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than solder. The standard height of the pillar (approx. 100um) adds to both the thermal and electrical resistance. Both bumping processes involve multiple processing steps and require specialized equipment which adds cost. The invention disclosed here is shown in Figure 3. Solderable metal contact regions are formed directly onto the top metal surface of the die. The solderable metal regions allows the die to be directly soldered onto a printed circuit board. Advantages of this system is that it requires only the deposition and patterning of thin metal layers on the order of 1um thick. Examples of solderable films are TiCu, TiNiAg, or AlNiVCu. These films can be used alone or covered with a top layer of solder. The solder layer will help to prevent oxidation of the exposed metal and may simplify mounting to the printed circuit board.

The die with a solderable metal system can be mounted to the printed circuit board using conventional surface mount techniques. A thin layer of solder paste can be deposited with a stencil onto the printed circuit board. The die is then placed into the proper location and lowered until it is in contact with paste. The printed circuit board assembly is then heated to approximately 200C until the solder reflows. The solderable metal patterns on the die are then directly soldered to the copper printed circuit board traces thereby forming a mechanical, electrical, and thermal connection. A illustration of a die mounted onto the printed circuit board is shown in Figure 4.

If the optional solder layer is added to the solderable metal system, it is not necessary to apply the solder paste. The solder on the die, once reflowed, will be sufficient to attach the die to the printed circuit board, further simplifying the assembly process.

Advantages of this invention are summarized as follows:

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Simplicity of the packaging

Ease of manufacturing

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Simplicity of mounting device to the printed circuit board

Enhanced thermal performance of the package.

Very short thermal path from the semiconductor die to the printed circuit board.

Contact areas can be maximized to increase area of thermal path thereby reducing the thermal resistance

Very low electrical resistance from die surface to the printed circuit board.

Short current path from die to printed circuit board.

Contact areas can be increase to further minimize the series resistance.

No wire bond or lead frame inductance and resistanc

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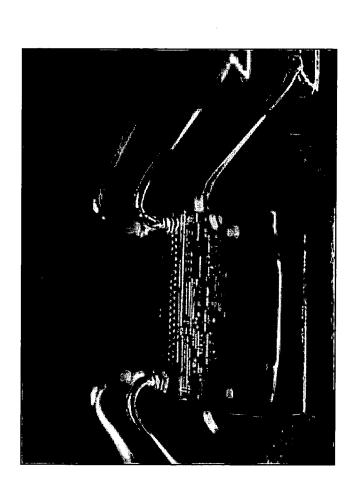


Figure 1. Example of Wire Bonding Used to Form the Electrical Connections to the Semiconductor Die

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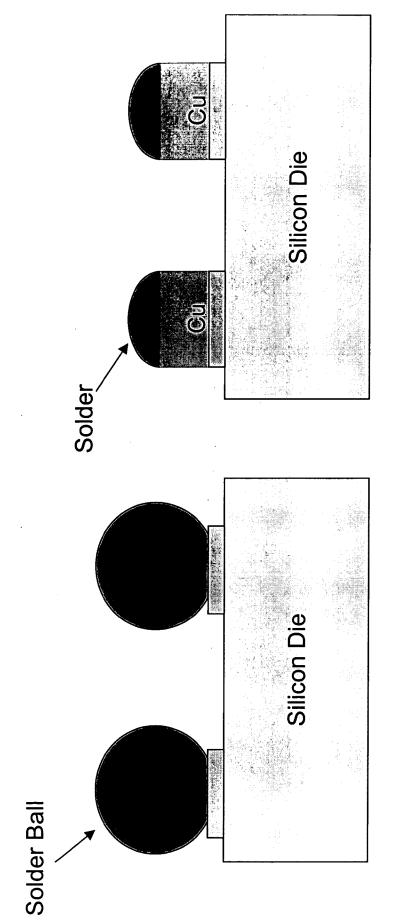
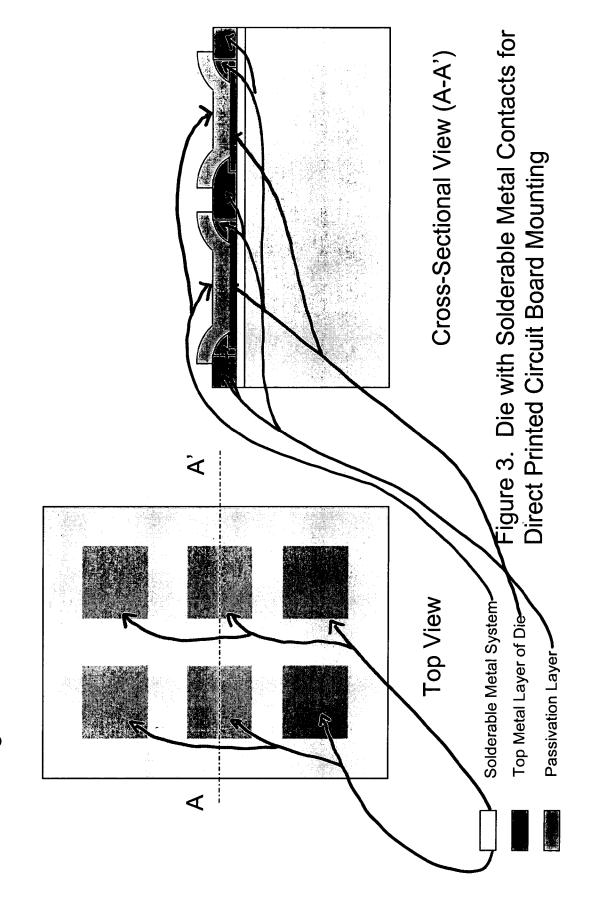


Figure 2. Typical Flip Chip Wafer Bumping Packages

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